How to Design a 98% Efficient, 3 kW 2-phase, 3-level Converter Using Paralleled eGaN® FETs

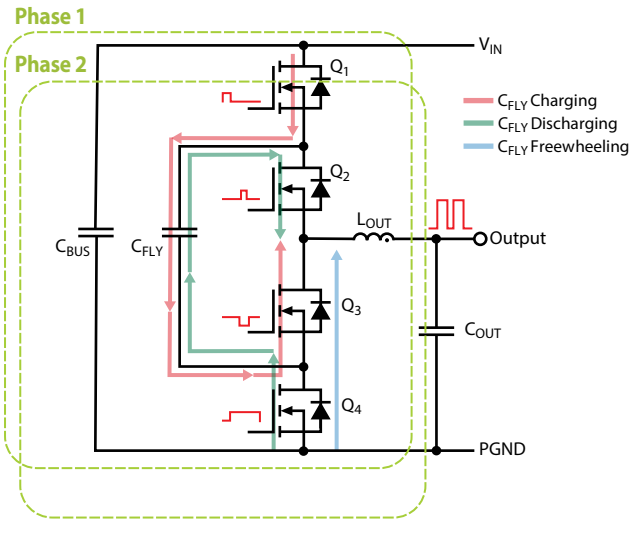
Motivation

As the revolution of renewable energy as well as transportation electrification progresses, the need for residential energy storage systems are increasing. A high efficiency DC-DC converter is usually required to exchange energy generated from renewable sources, such as solar panels with a battery. The fast-switching speed and low $R_{DS(on)}$ of eGaN FETs can help save energy by reducing power consumption inside the DC-DC converter[1]. This application note shows how to design a 98% efficient 100–250 V to 40–60 V DC-DC converter taking advantage of the low $R_{DS(on)}$ of **EPC2215**. A 3-level topology offers a 2x reduction of voltage and current stresses, which improves overall efficiency.

Advantages of a 3-level buck or boost converter

The 3-level flying capacitor buck or boost converter is an attractive topology as it allows for a 2x reduction in both voltage and volt-seconds stress on the inductor, as well as 4x inductance reduction compared to a conventional two-level converter with the same current ripple [2]. Figure 1 shows the operation of the three-level converter in buck mode. One top switch and one bottom switch forms two complementary switch pairs Q_1/Q_4 and Q_2/Q_3. Top switch Q_1 and Q_2 operate at the same duty cycle but have a 180° phase shift between them, while the bottom switch Q_3 and Q_4 operate at a complementary duty cycle.

The conventional current mode control can still be applied for this converter, as shown in figure 2. In such configuration, the output voltage loop generates the reference for the inner current loop. To ensure the switches have even voltage stress ($0.5 \cdot V_{IN}$) when the switch is off, an additional flying capacitor voltage loop is added to actively regulate the flying capacitor voltage, this can be achieved by adjusting the charging and discharging period of the flying capacitor [3].



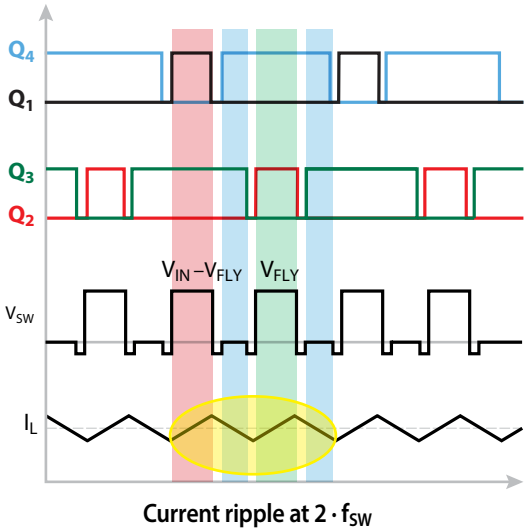
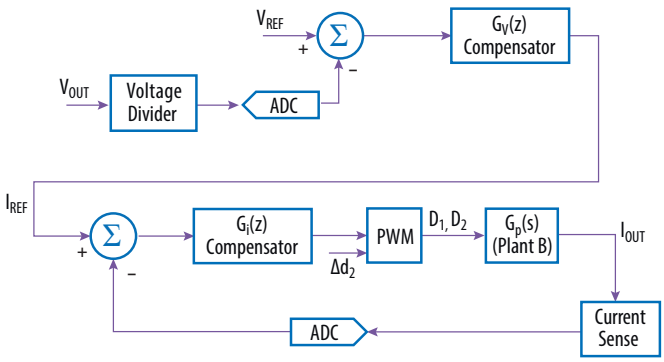


Figure 1. Operation principal of the three-level converter when $V_{OUT}/V_{IN} < 0.5$



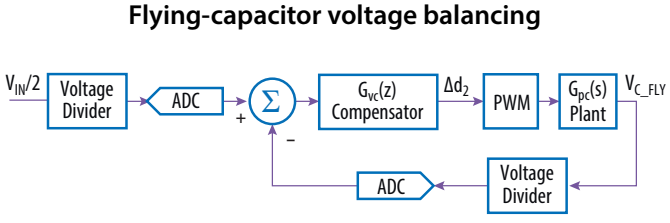


Figure 2. Block diagram of output voltage and flying capacitor voltage balancing control loop

Experimental Validation

A 3 kW capable experimental 2-phase (1.5 kW single phase) 100 V–250 V input and 40 V–60 V output 3-level DC-DC converter, ideal for battery charger applications in energy storage systems was built and tested as shown in Figure 3. It can supply up to 60 A into a 48 V load and achieve 98% peak efficiency at 250 V input and 40 V output. The experimental unit comprises two interleaved phases and each phase employs a three-level flying capacitor converter topology designed using two **EPC2215 FETs** [4] connected in parallel for each switch position and operated at 150 kHz switching frequency.

Each phase employs three half-bridge gate drivers NCP51820 [5]. One gate driver drives Q_3 and Q_4. To drive the upper switches of Q_2 and Q_1, two additional high-side gate driver output are used. The gate drivers are powered by a cascaded boot strap circuit. A zoomed-in layout of the switch and capacitor placement is shown in Figure 4. Low ESL ceramic capacitors are placed between switch pair Q_1/Q_4 and Q_2/Q_3 which acts as high frequency decoupling paths to reduce the parasitic inductances associated with each switch positions.

The experimental unit is digitally controlled. The experimental unit is tested with the input on the high voltage port and output voltage regulated down to 40 V. In this mode, the controller is comprised of one single output voltage loop, two current loops and two flying capacitor balancing loops as shown in figure 2. The two current loops share the same current reference generated by the output voltage side to ensure active current balancing. The two phases are interleaved (180-degree phase shift) to achieve ripple canceling on the high voltage side.

Measured waveform is shown in Figure 5 which shows the switch node of one phase at 24 A output with V_{OUT} = 40 V and V_{IN} = 200 V . Measured efficiency and loss at V_{OUT} = 40 V and V_{IN} = 200 V are given in Figure 6. In single phase configuration, the converter achieves 98% peak efficiency around 14 A output .

The experimental board is equipped with an aluminum heat-spreader and heatsink which can be attached to the back side of the PCB where the FETs are located. The heat-spreader is mounted to the PCB using SMD threaded spacers which are 1mm tall and use 6 mm long M2 countersunk screws for a flat mounting surface and follow best practice [6]. High performance thermal interface material (TIM) from T-Global (part TG-A1780) is used between the FETs and heat spreader for improved heat conductance. A heatsink is attached to the flat mounting face of the heatspreader. A two-part gap filler TIM (Bergquist GF4000) is used for the thinnest bond line thickness, and to provide some adhesion between the heatsink and heat-spreader. With this cooling method, Figure 7 shows temperature measurements taken from the top side of the PCB with IR camera and only a 30°C temperature rise is recorded. The air flow used is around 1500-2000 LFM.

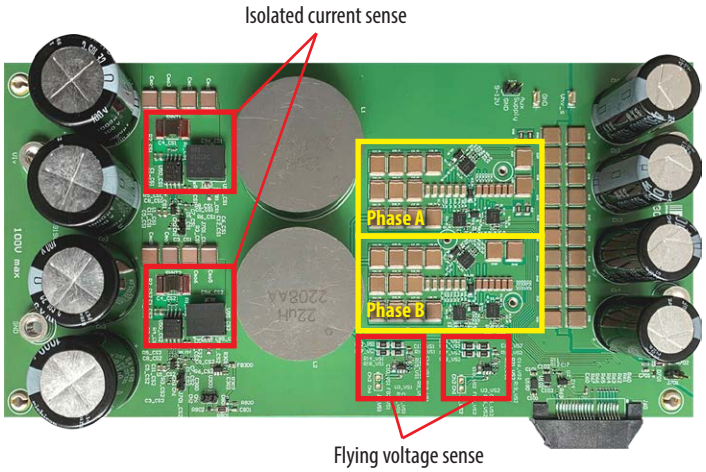


Figure 3: The experimental unit image with identification of that various function circuits

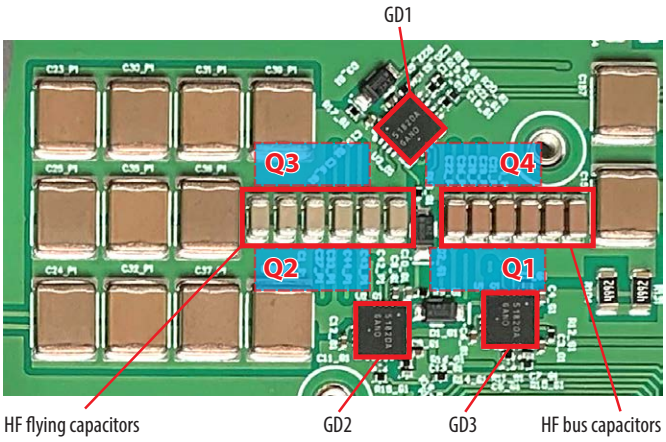


Figure 4: A zoomed in layout of the power stage area showing switches (Q_1-Q_4 located on the bottom side of the PCB), gate drivers (GD1-3) and capacitor placement

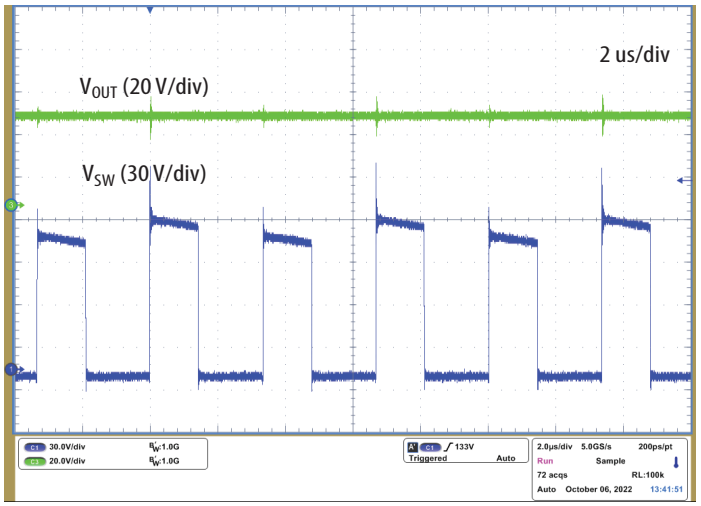


Figure 5: Typical switch node waveforms showing several switching cycles when the board is operating from 200 V input and delivering 24 A into a 40 V load.

In this application note, the design of a 3 kW two phase (1.5 kW single phase) DC-DC converter reference design using eGaN® FETs EPC2215 is presented. A three-level topology is used which allows for 2x reduction in current and voltage stresses in the switches. In experiment, 98% efficiency is achieved at 200 V input and 40 V output. The temperature rise of the FET is around 30 degrees Celsius with top side cooling using a heatspreader and heatsink.

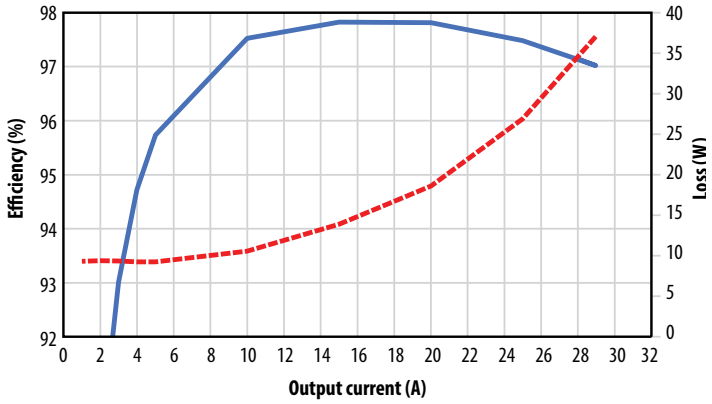


Figure 6: Measured efficiency (left axis) and power losses (right axis) with V_{OUT} = 40 V and V_{IN} = 200 V

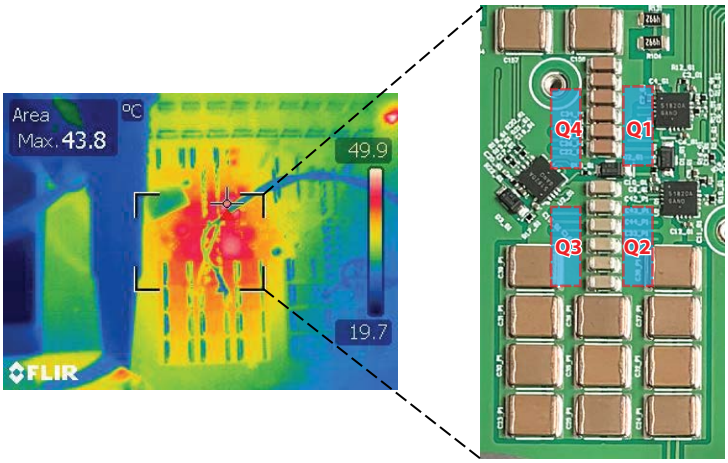


Figure 7: Thermal image taken from the top side of the PCB when operating from 200 V input and delivering 24 A into 40 V load in an ambient of 20°C

References

[1] A. Lidow, M. De Rooij, J. Strydom, D. Reusch, and J. Glaser, GaN Transistors for Efficient Power Conversion, 3rd ed. John Wiley & Sons, 2019. ISBN: 978-1119594147.

[2] T. A. Meynard and H. Foch, "Multi-level conversion: high voltage choppers and voltage-source inverters", PESC '92 Record. 23rd Annual IEEE Power Electronics Specialists Conference, vol. 1, pp. 397-403, June 1992.

[3] B. P. McGrath and D. G. Holmes, "Analytical modelling of voltage balance dynamics for a flying capacitor multilevel converter", IEEE Transactions on Power Electronics, vol. 23, no. 2, pp. 543-550, March 2008.

[4] EPC2215 – Enhancement Mode Power Transistor - EPC-co.com (no date). Available at: https://epc-co.com/epc/Portals/0/epc/documents/datasheets/EPC2215_datasheet.pdf (Accessed: November 29, 2022).

[5] NCP51820 - high speed half-bridge driver for Gan Power Switches - Onsemi (no date). Available at: https://www.onsemi.com/pdf/datasheet/ncp51820-d.pdf (Accessed: November 29, 2022).

[6] How2AppNote012, Thermal Management of eGaN® FETs- EPC-co.com. Available at https://epc-co.com/epc/Portals/0/epc/documents/application-notes/How2AppNote012%20-%20How%20to%20Get%20More%20Power%20Out%20of%20an%20eGaN%20Converter.pdf